

# Power Management in Portable ARM based Systems

Cliff Brake  
2002-12-11

## 1 Abstract

*As many computing systems are now portable, power management is a regular part of many ARM based systems. ARM based processors are especially well suited to portable systems because they provide a high level of performance at very low power. System issues are also important for an effective power managed system. This paper provides an overview of the hardware and system power management issues.*

## 2 Power Management

Power management is the effort to minimize power usage in a portable system. The primary benefit is increased battery life, but there are other benefits such as reduced heat dissipation. It is important to understand where the power in a system is going and where efforts to reduce power can be best spent. Illustration (1) is an example power distribution for a PDA class device. Power management is a system issue as the software, processor, peripherals, and power supplies must work together to effectively manage power.

## 3 Processor

The processor in a portable system contains a significant number of switching transistors relative to the rest of the circuitry in the system; therefore it uses a significant amount of power. Because a processor runs software, it is possible to know when parts of the processor can be shut down or slowed down when they are not needed.

### 3.1 CMOS Basics

Processors are manufactured using CMOS circuits. The following equation illustrates the relationship between Power  $P$ , CMOS gate capacitance  $C$ , switching frequency  $f$ , and supply voltage  $V$ .

$$P = C \cdot f \cdot V^2 \quad (1)$$

The CMOS gate capacitance  $C$  is fixed for a particular processor, but switching frequency  $f$  and supply voltage  $V$  can typically be adjusted to suit the application. There is another relationship between supply voltage  $V$  and switching frequency  $f$  that must be considered. Higher switching frequencies require higher supply voltages (2).

$$V \propto f \quad (2)$$

Power Distribution in a PDA class sample device

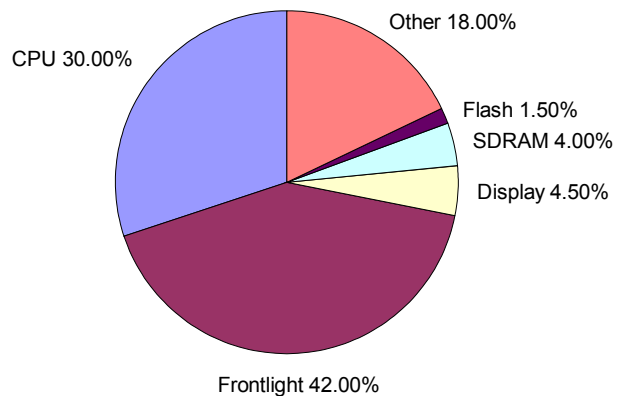


Illustration (1)

Processor manufacturers typically specify several operational voltage and frequency combinations.

### **3.2 Processor Idle Mode**

Almost all modern processor designs support an *idle mode*. During the idle state, the clock to the processor core stops, reducing the power used when the processor is not busy. The processor is put in the idle state by the operating system kernel when it determines there are no active tasks. The processor “wakes up” from the idle state when any system interrupt occurs. As most systems have an OS timer interrupt running, the processor may go into the idle state thousands of times per second.

It is important to note that the processor idle mode only affects the processor and has no effect on other hardware components in the system.

### **3.3 Voltage and Frequency Scaling**

There has been some interest in dynamic frequency and voltage scaling. From a pure CMOS perspective, there is little benefit to reducing frequency by itself, as the power required per instruction is still the same. The idle state is the reason reducing switching frequency alone will not save power. With higher switching frequencies, the processor simply gets its work done quicker and spends more time in the idle state. However, if voltage is reduced as well as frequency, the power per instruction is reduced. Because voltage  $V$  is a quadratic relationship with power  $P$ , small reductions in voltage result in significant amounts of power. Reducing the voltage by 29% will result in a 50% reduction in power.

From a system perspective, there may be some benefit to scaling frequency. There is research [2] that suggests that batteries do not operate efficiently when the power demand is not constant and has high peaks. A system spending a lot of time in the *idle mode* may present this scenario, depending on the battery technology and the power supply filtering relative to how frequently the system enters the idle mode. Careful system analysis and testing is

required to determine if there is any benefit to dynamically scaling only the frequency.

Scaling both voltage and frequency is a technique currently used with PC notebook class processors [1]. Although a processor manufacturer may specify several voltage/frequency operating points, it is very important that dynamic requirements also be specified if the voltage and frequency are going to be changed at run time. The power supply slew rate must be carefully controlled to meet the processor specification and parts of the processor may have to be disabled during a frequency change.

Recent announcements from ARM and National Semiconductor indicate that voltage technology may eventually be integrated directly on the processor. The circuitry on the processor will look at frequency, temperature, and process variations to optimally determine the required voltage instead of using worst case values.

### **3.4 Processor Peripherals**

Most ARM based processor include a significant number of peripherals on-chip. If a peripheral is not being used, the clock to the peripheral should be stopped if possible. Circuitry supporting the peripheral may also be powered off if control is available.

## **4 System Issues**

Illustration (2) shows the basic system power managements states.

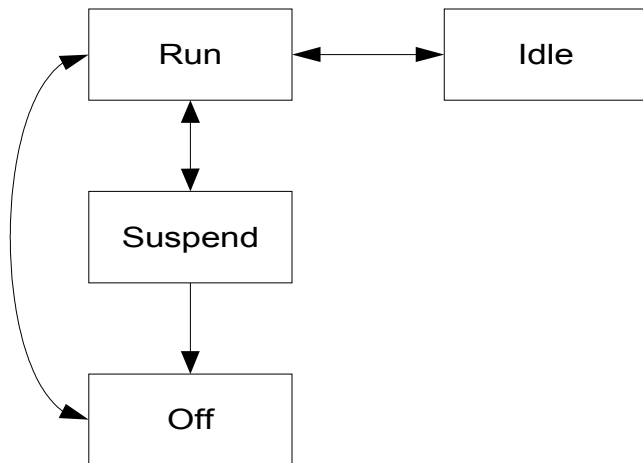


Illustration (2)

## 4.1 System Suspend

During the system suspend (also called sleep) state, only the following components are left powered up.

- SDRAM
- Processor Power Management Circuitry
- Wake circuitry

Because the SDRAM contents are preserved, the application state of the system is preserved. The following steps typically occur to enter sleep mode:

1. User, timeout, or low battery situation initiates the suspend sequence.
2. The OS makes calls to each device driver to put the hardware peripheral into a low power state.
3. Processor registers that are not preserved during suspend are saved to SDRAM.
4. The SDRAM is put into a self refresh mode.
5. The processor is put into the suspend mode. In this mode, the clock to the processor core is stopped, and various power supplies in the system are powered down.

The resume sequence is the opposite of the suspend sequence and is initiated by a wake pin on the processor or an internal processor wake source such as a real time clock alarm. Implementing the suspend mode in a system is a big task as it requires an understanding of all the peripherals in the system and how to transition them to a low power state.

For a PDA class device, the suspend mode power is on the order of 10mW. A PDA class system can transition between the run and suspend state in 10's of mS – near instant from a human perspective.

## 4.2 System Off

Even with the reduced power used in suspend state, a PDA class system will only last at most a couple weeks in suspend mode. It is often desirable to have an *OFF* mode (also called ship) that uses virtually no power. This mode is useful to avoid damage to the batteries when the battery is dead and also for shipping so a device can be shipped or stored with the battery installed.

## 4.3 Soft Reset

Most systems require a soft (warm) reset functionality where the system processor can be reset, but the SDRAM contents are preserved. As many portable systems store user files in RAM, this is a nice feature.

# 5 Hardware

There are a number of specific hardware aspects that can be considered for power management.

## 5.1 Display and Frontlight

The display typically consumes the most energy in a PDA class system. There are a number of displays available, but most modern PDA use some type of reflective TFT display with a frontlight. Although a reflective TFT screen can be read in bright light without a frontlight, a frontlight is required most of the time for comfortable viewing. There are two types of frontlight used:

- CCFT (Cold Cathode Fluorescent Tube)
- Side mounted LEDs

LED frontlights use less power, but there are other tradeoffs to be considered.

It is common for portable system software to dim the frontlight if there is no user input for a short period of time. For certain applications (such as music playback), it may be acceptable to disable the entire display.

### 5.2 Lower Power SDRAM

Many systems can use low power SDRAM which runs at 2.5 or 1.8 volts versus the conventional 3.3 volts. Table (1) compares power used by 64MBytes of ram in a 3.3V and a 1.8V system. The data for the calculations was obtained from Micron datasheets for 256Mbit SDRAM components [3] [4]. The run (100% duty cycle) and suspend power for one device is multiplied by two as two devices are required.

<i>Ram Type</i>	<i>Run Power mW</i>	<i>Suspend Power mW</i>
Normal (3.3V)	891	9.9
Low Power (2.5)	324	1.26

Table 1

Going from 3.3V to 1.8V will significantly increase the run time and suspend time of a portable system.

SDRAM components support several low power states. The SDRAM Self-Refresh state is used during the system suspend state. During this state, all signals to the SDRAM are inactive except for CKE, and the SDRAM manages its own refresh. SDRAM components also support a power-down mode that can be used while the system is in the run or idle state.

### 5.3 Audio

Audio components that have a low power mode (in the  $\mu$ A range) should be selected. Otherwise, the

power must be switched off to the devices in the suspend state. Care must be taken when transitioning power in audio circuits to avoid undesired audio artifacts such as popping noises.

### 5.4 Power Supplies

Power supply IC vendors continue to make advancements. Modern switching supplies switch in the MHz range which reduces the size of capacitors and magnetics required in the circuit. At high switching frequencies, extra care must be taken in the layout so the power supply control loop works properly. If a switching power supply is to be left running in the suspend state, it should support a low power mode where it can supply the very low suspend power at reasonable efficiency. These are often referred to as dual mode switching power supplies.

### 5.5 Backup Power Source

If the system has a removable main battery, some type of backup power source should be considered. This backup power source keeps the system alive in the suspend state while the main battery is being replace. Most PDA class systems require a battery for the backup power source due to the power required in the suspend state.

### 5.6 Critical Events

Hardware support for several critical events is usually required. The first critical event can be called *critical battery*. In this state, the OS must be notified that the battery is critically low and the OS will then unconditionally transition the system to the suspend state. The other critical state can be called *dead battery*. In this state, the battery is not completely dead, but further discharge must be prevented to avoid damaging the battery. This state is handled by a small amount of extremely low power hardware circuitry that detects the state and disconnects the main battery from the system. All SDRAM contents are lost when this critical event occurs.

## 5.7 Sourcing Issues

Sourcing issues are probably the number one hardware problem encountered when trying to get a system to suspend (power down) properly. Sourcing occurs when an IC is in a powered down state but one of the input signals is left in a high state. If the IC has protection diodes on the inputs, current will be directed through the protection diode to the IC power pins as shown in Illustration (3). This causes the power supply voltage to increase to some indeterminate level and results in relatively large amounts of power being dissipated when the system should be using very little power. The solution for this problem is to make sure input signals to ICs (that have protection diodes) are in a low state before powering down the IC. Signals that cannot be driven low in the suspend state may have to be buffered.

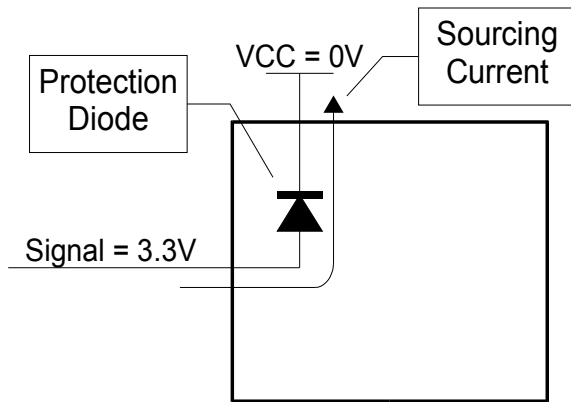


Illustration (3)

## 6 Summary

Power management in a portable device is a system issue. A successful design requires a thorough understanding of the system and attention to many details.

## 7 Acknowledgments

I thank the Engineering staff at Accelent, of which I am part of, for contributing information for this paper.

## 8 References

- [1] M. Fleischmann, "LongRun Power Management", Transmeta Corporation, Jan. 2001.
- [2] T. Martin, "Balancing batteries, power, and performance: system issues in CPU speed-settings for mobile computing", PhD. Dissertation, Carnegie Mellon University, Aug. 1999.
- [3] Micron Datasheet, "256Mb SDRAM", Micron Technology, Inc., 2001.
- [4] Micron Datasheet, "256Mb MOBILE SDRAM", Micron Technology, Inc., 2002.